UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,521	01/27/2004	Gabriele Gandolfi	853063.508	2210

38106 7590 02/03/2005

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,521	GANDOLFI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. It appears that Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). As applicant indicates in the specification that the embodiment of the present invention provides a control switch that has a resistance modulation which is reduced in comparison with the known art (lines 12-14 on page 2 of the instant specification), and applicant also clearly recites that the resistance variation for the switch circuit of Figure 1 is 30% which cannot be compatible with some design requirements and therefore an improved switch circuit of Figure 2 is designed/invented (see lines 14-22 on page 4 of the instant specification). Thus, it appears that Figure 1 should be labeled as --Prior Art--.

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1, 2 and 5 are objected to because of the following informalities:

Claim 1, line 2, "controlled" should be changed to --control--.

Claim 2, lines 2 and 3, it is suggested to changed "present" to --active--.

Claim 5, lines 4, 5, 7, 8 and 9, it is suggested to changed "applied" to --connected--.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 and 12-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "said switch" on line 2 lacks antecedent basis and it is not clear whether it refers to the controlled switch recited earlier in the claim. Further, the phrase "a control circuit ... a MOS transistor" recited on line 2-5 is indefinite because it is not clear whether "a MOS transistor" (line 5) is the same as "said switch" (line 2) and "said controlled switch" (lines 3 and 4). It is clearly from the operation of the circuitry (Figure 2) that the control circuit (S1, S2, C, M6-M8) is for controlling the on/off of the MOS transistor (M1). To overcome the indefiniteness of claim 1, it is suggested to change "said switch" on line 2 to --a MOS transistor--; "controlled switch" on lines 3 and 4 to --MOS transistor--; and "a MOS" on line 5 to --wherein said MOS--.

Claims 2-5 are indefinite because they include the indefiniteness of claim 1.

With respect to claim 12, the recitation "the fifth and sixth switches being controlled by a first control signal" recited on line 3 is indefinite because it is inconsistent with what is shown and disclosed. It is disclosed in Figure 2 that the only the switch (S2) is controlled by the first control signal and the fifth switch (M6) is not control by the first control signal since the control terminal of the fifth switch is connected to the control terminal of the first MOS transistor (M1). Clarification and/or appropriate correction is required.

Claim 13 is indefinite because it includes the indefiniteness of claim 12.

With respect to claim 14, the recitation "the fourth switch is an NMOS transistor" on line 1-2 is misdescriptive since it is inconsistent with what is disclosed and shown. It is clearly disclosed in Figure 2 that the fourth switch (M7) which connected between the second terminal of the capacitor (C) and the gate of the first MOS transistor (M1) is a PMOS transistor, not an NMOS transistor. Clarification and/or appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 6-9, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shigehara et al. (USP 6,462,611).

Insofar as understood in claim 1, Figure 3 of the Shigehara et al. discloses a switching circuit, which includes: a control circuit (INV1, INV2, COMP-N2) for a MOS transistor (N1), in a first phase (VGN = LO, VGP = HI) the controlled circuit opens the MOS transistor (N1), in a second phase (VGN = HI, VGP = LO) the controlled circuit closes the MOS transistor (N1); wherein the MOS transistor (N1) having a source (at input B) and a bulk (body), wherein in the first phase (VGN = LO, VGP = HI) the bulk is electrically connected to ground (transistor N2 is ON) and in the second phase the bulk is coupled to the source (transistors N1N and P1N are ON).

With respect to claim 2, in the first phase a first control signal (VGP) is active, and in the second phase a second control signal (VGN) is active.

With respect to claim 3, Figure 3 shows the bulk is coupled to ground by a switch (N2) controlled by the first control signal (VGP).

With respect to claim 4, Figure 3 shows the bulk is coupled to the source by a switch (P1N, N1N) controlled by the second control signal (VGN).

With respect to claims 6 and 7, Figure 3 shows a first MOS transistor (N1) having a source (B), a drain (A), a gate, and a bulk (body), wherein the source and drain are connected between the input (B) and output (A); a first switch (N2) connected between the bulk and a first reference voltage (ground); and a second switch (N1N, P1N) connected between the bulk and the input (B).

With respect to claim 8, it is seen in the operation of Figure 3 that the first switch (N2) is controlled by a first control signal (VGP) and the second switch (N1N, P1N) is controlled by a second control signal (VGN), wherein the first and second control signals having non-overlapping active phases (because the two signals are inverted of each other) such that the second switch is open while the first switch is closed and vice versa.

With respect to claim 9, Figure 3 shows the second switch (N1N, P1N) includes complementary second and third MOS transistors (N1N, P1N) connected in parallel between the bulk of N1 and the input B, the second MOS transistor (N1N) is controlled by a control signal (VGN) and the third MOS transistor (P1N) is controlled by an inverted form of the control signal (VGN).

With respect to the method claims 15 and 16, Figure 3 discloses a switching circuit that meets all the limitations of the apparatus claims as discussed above with respect to claims 1-4 and 6-9. Hence, it also deems to meet all the method steps recited in claims 15 and 16.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 6-10, 12, 13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pinna et al. (US 2002/0021162 A1) in view of Shigehara et al. (USP 6,462,611).

With respect to claim 1, Figure 5 of the Pinna et al. reference discloses a switching circuit, which includes: a MOS transistor (64) and a control circuit (all elements in Figure 5 except for the MOS transistor 64) for controlling the MOS transistor (64) wherein in a first phase (F2D = Hi) the control circuit opens the MOS transistor (64), an in a second phase (F1D = Hi) the control circuit closes the MOS transistor (64). Figure 5 of the Pinna et al. reference does not disclose that the bulk of the bulk of the MOS transistor is connected to ground while the MOS transistor is opened (the first phase) and is connected to the source of the MOS transistor while the MOS transistor is closed (the second phase). However, the Shigehara et al. reference discloses in Figure 3 a switching (M1, COMP-N2) includes a body effect compensation circuit COMP-N2 connected to the bulk and source of the MOS transistor M1 such that the bulk of the MOS transistor (M1) is connected to ground when the MOS transistor is opened (off) and is

connected to the source of the MOS transistor (at input B) when the MOS transistor is closed (on) for the purpose of increasing the operation speed (Col. 9, lines 37-45). Therefore it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 5 of the Pinna et al. reference by providing a body effect compensation circuit (COMP-N2, Figure 3 of Shigehara et al.) connected to the source and the bulk of the MOS transistor (64, Figure 5 of Pinna et al.), as taught by the Shigehara et al. reference, such that the bulk of the MOS transistor (64) is connected to ground when the MOS transistor is opened (off) and is connected to the source of the MOS transistor (at input B) when the MOS transistor is closed (on) for the purpose of increasing the operation speed (Col. 9, lines 37-45 of Shigehara et al.). Thus, this combination meets all the limitations of claim 1. Note that in this combination, the gate of the transistor N2 in the body effect compensation circuit (COMP-N2) would be controlled by signal F2D (first phrase), and the gates of the transistors N1N and P1N would be controlled by signals F1D and F1D/ (second phase)

With respect to claim 2, it is seen in the above combination that in the first phase the first control signals (F2D, Figure 5 of Pinna et al.) is active, and in the second phase the second control signal (F1D and F1D/, Figure 5 of Pinna et al.) is active.

With respect to claim 3, the switch is shown in the above combination (transistor N2 of the circuit COMP-N2 in Figure 3 of Shigehara et al.).

With respect to claim 4, the switch is shown in the above combination (transistors N1N and P1N of the circuit COMP-N2 in Figure 3 of Shigehara et al.).

With respect to claims 6-10, 12, 13, the above combination as discussed meets all the limitations of this claim, i.e., a first MOS transistor (64, Figure 5 of Pinna et al.), a first switch

(N2, Figure 3 of Shigehara et al.) controlled by a first control signal (F2D, Figure 5 of Pinna et al.), a first reference voltage (ground), a second switch (N1N and P1N, Figure 3 of Shigehara et al.) controlled by a second signal (F1D and F1D/, Figure 5 of Pinna et al.), a capacitor (68, Figure 5 of Pinna et al.), a third switch (84 and 86, Figure 5 of Pinna et al.), a fourth switch (NMOS 74, Figure 5 of Pinna et al.), a fifth switch (78, Figure 5 of Pinna et al.) connected between the second terminal of the capacitor (68) and a second reference voltage (Vcc), a sixth switch (80, Figure 5 of Pinna et al.), a seventh switch (76, Figure 5 of Pinna et al.).

With respect to the method claims 15-19, the combination as discussed above discloses a switching circuit that meets all the limitations of the apparatus claims as discussed above with respect to claims 1-4, 6-10, 12 and 13. Hence, it also deems to meet all the method steps recited in claims 15-19.

10. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA), Figure 1, in view of Shigehara et al. (USP 6,462,611).

With respect to claims 1-19, Figure 1 of Applicant's Prior Art (APA) discloses a switching circuit, which includes: a MOS transistor (M1) and a control circuit (all elements in Figure 1 except for the MOS transistor M1) for controlling the MOS transistor (M1) wherein in a first phase (F1 = Hi) the control circuit opens the MOS transistor (M1), an in a second phase (F2 = Hi) the control circuit closes the MOS transistor (M1). Figure 1 of the APA does not disclose that the bulk of the bulk of the MOS transistor is connected to ground while the MOS transistor is opened (the first phase) and is connected to the source of the MOS transistor while the MOS transistor is closed (the second phase). However, the Shigehara et al. reference discloses in Figure 3 a switching (M1, COMP-N2) includes a body effect compensation circuit COMP-N2

connected to the bulk and source of the MOS transistor M1 such that the bulk of the MOS transistor (M1) is connected to ground when the MOS transistor is opened (off) and is connected to the source of the MOS transistor (at input B) when the MOS transistor is closed (on) for the purpose of increasing the operation speed (Col. 9, lines 37-45). Therefore it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 1 of the APA by providing a body effect compensation circuit (COMP-N2, Figure 3 of Shigehara et al.) connected to the source and the bulk of the MOS transistor (M1, Figure 1 of APA), as taught by the Shigehara et al. reference, such that the bulk of the MOS transistor (M1) is connected to ground when the MOS transistor is opened (off) and is connected to the source of the MOS transistor (at input B) when the MOS transistor is closed (on) for the purpose of increasing the operation speed (Col. 9, lines 37-45 of Shigehara et al.). Note that in this combination, the gate of the transistor N2 in the body effect compensation circuit (COMP-N2) would be controlled by signal F1 (first phrase), and the gates of the transistors N1N and P1N would be controlled by signals F2 and F2N (second phase). Thus, this combination meets all the limitations of claims 1-19, including the method steps of claims 15-19, because the structure of this combination is substantially as the structure of the invention (Figure 2). Note that, for claims 1-5, the switch connected the bulk of M1 to ground is N2 (Figure 3 of Shigehara et al.), the switch connected the bulk of M1 to the source is transistors N1N and P1N (Figure 3 of Shigehara et al.), the control circuit (in Figure 1 of the APA) includes a first switch (S1), a capacitor (C), a second switch (S2), a third switch (M6), a prefixed reference voltage (Vref), a fourth switch (M7), and a fifth switch (M8); and for claims 6-14, the first MOS (M1, Figure 1 of APA), a first switch (N2, Figure 3 of Shigehara et al.), a first reference voltage (ground), a

second switch (N1N-P1N, Figure 3 of Shigehara et al.), and Figure 1 of the APA shows a first control signal (F1), a second control signal (F2), a capacitor (C), a third switch (S1), a fourth switch (M7), a fifth switch (M6), a second reference voltage (Vref), a sixth switch (S2), a seventh switch (M8).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 31, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816